Application Note

Anritsu

Evaluating Gbps Class Interconnects

Multilane Gbps Interconnects

MP1800A/MT1810A
Signal Quality Analyzer/4Slot Chassis

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Fabricating high-density, multilane, Gbps-class interconnects is a hot topic.

The spread of rich-content Internet services that support high-resolution graphics, video, and audio applications is not only driving increasing network transmission capacities, it is also accelerating the development pace of high-speed processing equipment.
Even the household computing environment has experienced the increasing adoption of Gbps-class devices in networking equipment, such as routers, storage, and servers. Progress in Gbps-class interconnects has also caused a stir in other application fields, such as supercomputers that require massive computation power. However, achieving Gbps-class speeds in future equipment is not just a matter of using Gbps devices, it also requires quick adoption of technologies supporting high-speed processing for PC boards (PCBs), too. Consequently, various Gbps-class standards are being adopted to achieve high-density, high-speed PCBs (Figure 1).

Comms Std	Bit Rate/Lane
PCI express	2.5 Gbit/s (Gen 1) 5.0 Gbit/s (Gen 2) 8.0 Gbit/s (Gen 3)
SATA	1.5 Gbit/s (Gen 1) 3.0 Gbit/s (Gen 2)
SAS	1.5 Gbit/s 3.0 Gbit/s 6.0 Gbit/s
Infiniband	2.5 Gbit/s
HDMI	3.4 Gbit/s
XAUI	3.125 Gbit/s

Figure 1. Main Serial Communications Standards

Developing these types of Gbps interconnects usually follows the design steps in Figure 2 below.

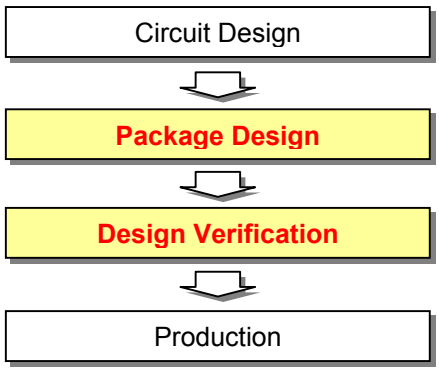


Figure 2. Development Stages

Both the package design and design verification stages require a multichannel BERTS that supports pattern synchronous measurements. This allows the verification of logic and package designs – from the perspective of the effects of signal separation, wiring lengths, adjacent signal crosstalk, PCB frequency characteristics, etc. – on output waveform quality. Currently, there are increasing problems with reduced transmission quality that results from adjacent signal effects in multilane PCBs, as well as problems with establishing compatibility. In addition, high-density designs have experienced drift, due to differences in lane wiring lengths, as well as drift in paired differential signals. High-speed signal transmission, frequency and data-pattern dependencies cause worries about reduced waveform quality. As a result, it is no longer sufficient to perform evaluations by measuring BER, jitter and waveform quality of each lane independently. Today's high-speed, multilane, serial communications standards require total evaluation of multilanes using a multichannel BERTS to perform the following quantitative measurements:

- **Waveform quality degraded by crosstalk**
- **Waveform quality degraded by synchronous switching**
- **Drift due to wiring lengths (interlane skew)**
- **Differential signal drift (differential skew)**
- **Degraded signal remedy (emphasis effect verification)**

Measurement Items and Methods for High-speed Serial Communications

Waveform Quality Degraded by Crosstalk

In Gbps-class interconnects, there is always concern about crosstalk that causes degraded waveform quality. Crosstalk pulses of several hundred ps are generated in adjacent lanes by lane signal switching. Since this is buried in the symbol width at low data rates it can be ignored. However, crosstalk pulses of several hundred ps cannot be ignored at Gbps data rates resulting in degraded waveform quality (S/N ratio).

Waveform Quality Degraded by Synchronous Switching

The rapid evolution in CMOS process technologies from 90 nm to 32 nm has caused orders-of-magnitude increases in the number of transistors on single chips of the same size. As a result, the number of synchronously switching transistors has also increased significantly, resulting in On/Off current fluctuations at synchronous switching and inviting reduced power supply transient response times.
Figure 3 shows an example of synchronous switching using the pattern sync function. The sync switching effect is measured by matching the pattern timing of the test signal input to each lane (Figure 3).

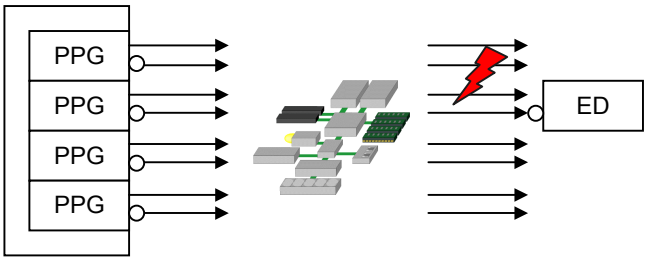


Figure 3. Crosstallk and Synchronous Switching Evaluation

Drift Due to Wiring Lengths (Interlane Skew)

Ideally, assuring that the sufficient margin in the Rx tolerance of ICs, such as SerDes, requires the same wiring length for each pattern of every lane. However, increasing demand for higher densities makes it difficult to assure that all patterns are precisely the same length. Also, Gbps-class patterns suffer from interlane skew that result from differences in the dielectric constant between PCB layers, making it difficult to determine the wiring length using only logic design. As a result, each Gbps-class interconnect standard specifies the interlane skew needed to prevent degraded margins, which cannot be ignored at operation testing (Figure 4).

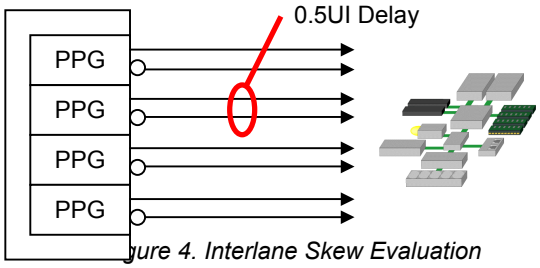
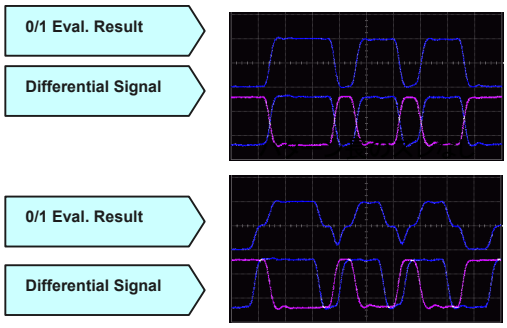


Figure 4. Interlane Skew Evaluation

Differential Signal Drift (Differential Skew)

To improve noise tolerance, Gbps-class interconnects use differential signalling with two signal lines for Data and xData. A disadvantage of this technique is that the bit margin is reduced when the respective phases drift due to differences in pattern length. For example, at a bit rate of 12.5 Gbit/s when the pattern length is 8 mm, the bit margin is halved if the phase drifts by 0.5UI (Figure 5).



0.5UI Drift at 8-mm Pattern Length and 12.5-Gbit/s Data Rate

Figure 5. Change in Differential Skew at Pattern Length Drift

Consequently, it is necessary to confirm the bit margin when the Data and xData skew changes (Figure 6).

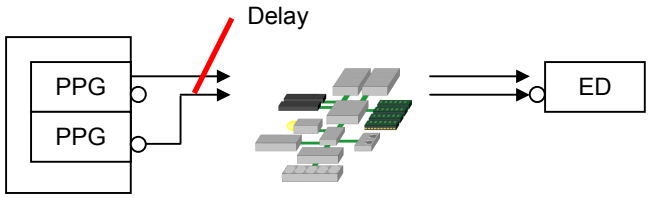


Figure 6. Differential Skew Evaluation

Degraded Signal Countermeasures (Emphasis Effect Check)

Even if the waveform is clean immediately after transmission, its amplitude decreases at the Rx point due to the PCB frequency characteristics and pattern length. The red waveform in Figure 7 shows how the eye pattern closes.

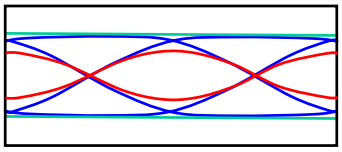


Figure 7. Signal Degradation due to Frequency Characteristics and Wiring Length

To prevent small amplitude and closed eye pattern, the transmission method emphasizes the 0→1 and 1→0 crossover points using a technique called Emphasis (Figure 8).

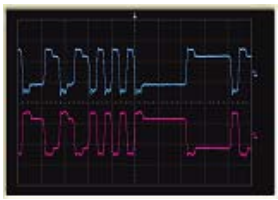


Figure 8. Emphasis Signal

Adding the correct degree of Emphasis to produce the optimum conditions at the Rx side requires analysis at package verification, to determine dependence on PCB characteristics, wiring length, etc. A multichannel BERTS supports generation of any Emphasis waveform by changing parameters on the frequency and time axes. Using this function supports verification of the optimum Emphasis waveform. Furthermore, performing separation analysis of the Transition and Non-Transition points at Eye Diagram measurement supports prompt troubleshooting of problems in the Emphasis waveform (Figures 9 to 11).

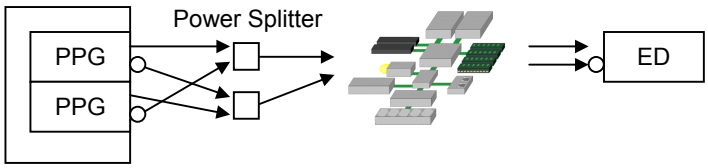


Figure 9. Emphasis Generation Method

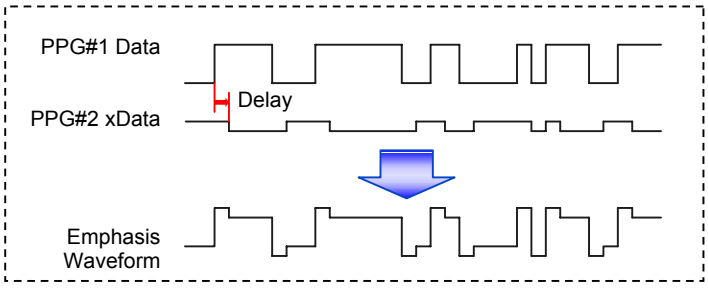


Figure 10. Principle of Emphasis Generation (Timing Chart)

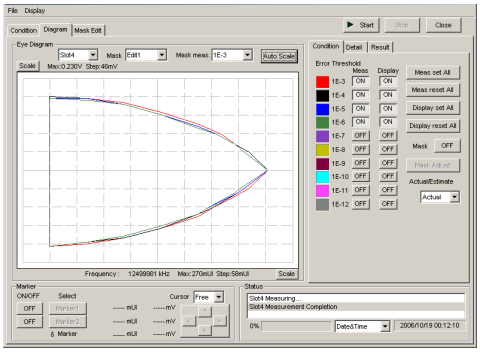


Figure 11. Separation Analysis using Eye Diagram (Non-Transition Waveform Eye Diagram Measurement Result)

Requirements for Pattern Sync Multichannel BERTS

Achieving the measurement items described in this leaflet requires a measurement instrument with a pattern synchronization function. Unlike bit synchronization, which only matches frequency, pattern synchronization matches the test signal start position (Figure 12). When using several separate PPG units, bit synchronization is possible but pattern synchronization is difficult (Figure 13).

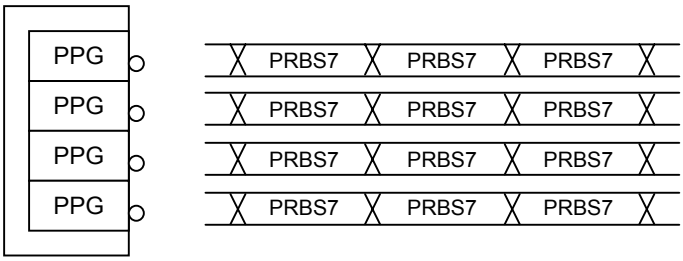


Figure 12. MP1800A Pattern Timing (Pattern Sync) when Transmitting PRBS7 on All Channels

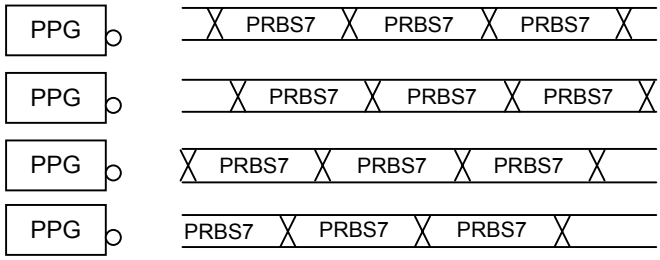


Figure 13. Pattern Timing for Multiple Separate PPG Units when Transmitting PRBS7 on all Channels

Summary

Anritsu's MP1800A/MT1810A is a modular-type multichannel BERT platform supporting installation of multiple PPGs and EDs. As a result, it supports the required test items explained in this leaflet with an easy to use pattern synchronization function.
Using this evaluation prevents the need for repeated evaluations, which shortens test times and increases product quality.

Glossary of Terms

Differential Signal
In differential signalling, when one signal swings to the positive side, the other signal swings simultaneously to the negative side. As a result, the Rx circuit cancels the common mode voltage and recognizes only the difference between the two signals. Consequently, external noise has the same impact on both signal lines, reducing the effect of electrical noise by ignoring common mode noise.

Crosstalk
This phenomenon is the result of an undesired signal leaking from one circuit to another. As an example, one signal is affected by another signal, resulting in mixed reception of the other signal.

Emphasis
This is a method for amplifying a data signal by compensating transmission loss caused by the transmission medium. The transition points (0→1 and 1→0) are amplified to the original signal.

Transition/Non-Transition Errors
Transition error occurs at transition bits (0→1 and 1→0). Non-Transition error occurs at consecutive strings of 0s or 1s without a bit transition.

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Specifications are subject to change without notice.

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